

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	§	
Wen-Chin Lin, et al.	§	Attorney Docket No.: 2003-0276
	§	(24061.163)
	§	
Serial No.: 10/780,171	§	Group Art Unit: 2824
	§	
Filed: February 16, 2004	§	Examiner: Sofocleous, Alexander
	§	
For: Segmented MRAM Memory Array	§	Conf. No.: 1738
	§	

Commissioner for Patents
Mail Stop RCE
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT FOR RCE

Sir:

No fees, including extension of time fees, are believed necessary for consideration of the present paper. However, if any fees, including extension of time fees, are necessary, the extension of time is hereby requested, and the Commissioner is hereby authorized to charge any fees, including those for the extension of time, to Haynes and Boone, LLP's Deposit Account No. 08-1394.

Please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on **page 2** of this paper.

Remarks begin on **page 7** of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-9 (Cancelled).

10. (Currently Amended) An MRAM memory array, comprising:

word lines;

bit lines crossing the word lines;

first diodes, each first diode comprising:

a cathode; and

an anode coupled to a corresponding bit line;

second diodes, each second diode comprising:

an anode; and

a cathode coupled to a corresponding word line; and

magnetic tunnel junction memories including:

a pinned layer;

a free layer; and

a non-magnetic layer located between the pinned layer and the free layer;

~~each magnetic tunnel junction memory being positioned at a crossing point of a bit line and a word line,~~ each magnetic tunnel junction memory being connected between a first diode at [[a]] the corresponding crossing bit line and a second diode at [[a]] the corresponding crossing word line.

11. (Original) The MRAM memory array as claimed in claim 10, wherein the number of diodes is equal to the total number of word lines and bit lines.

12. (Original) The MRAM memory array as claimed in claim 10, wherein the number of magnetic tunnel junction memories is the product of the number of word lines and the number of bit lines.

13. (Original) The MRAM memory array as claimed in claim 10, wherein the numbers of word lines is three and the numbers of the bit lines is two.

14. (Original) The MRAM memory array as claimed in claim 10, wherein the numbers of word lines is three and the number of bit lines is three.

15-16 (Cancelled).

17. (Currently Amended) An MRAM memory array, comprising:
- a first word line;
 - a second word line;
 - ~~a third word line;~~
 - a first bit line crossing the first word line, ~~the first bit line further crossing the~~ second word line, ~~the first bit line further crossing the third word line;~~
 - a second bit line crossing the first word line, ~~the second bit line further crossing~~ the second word line, ~~the second bit line further crossing the third word line;~~
 - a first diode having a first cathode, and a first anode coupled to the first bit line;
 - a second diode having a second cathode, and a second anode coupled to the second bit line;
 - a third diode having a third anode, and a third cathode coupled to the first word line;
 - ~~a fourth diode having a fourth anode, and a fourth cathode coupled to the second word line;~~
 - ~~a fifth diode having a fifth anode, and a fifth cathode coupled to the third word line;~~
 - a first magnetic tunnel junction memory connected between the first cathode and the third anode, the first magnetic tunnel junction memory including:
 - a first pinned layer;
 - a first free layer; and

a first non-magnetic layer located between the first pinned layer and the first free layer;

the first magnetic tunnel junction memory being ~~positioned at a crossing point of the first bit line and the first word line~~ connected between the first diode and the third diode;

a second magnetic tunnel junction memory connected between the second cathode and the third anode, the second magnetic tunnel junction memory including:

a second pinned layer;

a second free layer; and

a second non-magnetic layer located between the second pinned layer and the second free layer;

the second magnetic tunnel junction memory being ~~positioned at crossing point of the second bit line and the first word line~~ connected between the second diode and the third diode;

~~a third magnetic tunnel junction memory connected between the first cathode and the fourth anode, the third magnetic tunnel junction memory including:~~

~~a third pinned layer;~~

~~a third free layer; and~~

~~a third non-magnetic layer located between the third pinned layer and the third free layer;~~

~~the third magnetic tunnel junction memory being positioned at crossing point of the first bit line and the second word line;~~

~~a fourth magnetic tunnel junction memory connected between the second cathode and the fourth anode, the fourth magnetic tunnel junction memory including:~~

~~a fourth pinned layer;~~

~~a fourth free layer; and~~

~~a fourth non-magnetic layer located between the fourth pinned layer and the fourth free layer;~~

~~the fourth magnetic tunnel junction memory being positioned at crossing point of the second bit line and the second word line;~~
~~a fifth magnetic tunnel junction memory connected between the first cathode and the fifth anode, the fifth magnetic tunnel junction memory including:~~
~~a fifth pinned layer;~~
~~a fifth free layer; and~~
~~a fifth non-magnetic layer located between the fifth pinned layer and the fifth free layer;~~
~~the fifth magnetic tunnel junction memory being positioned at crossing point of the first bit line and the third word line; and~~
~~a sixth magnetic tunnel junction memory connected between the second cathode and the fifth anode, the sixth magnetic tunnel junction memory including:~~
~~a sixth pinned layer;~~
~~a sixth free layer; and~~
~~a sixth non-magnetic layer located between the sixth pinned layer and the sixth free layer;~~
~~the sixth magnetic tunnel junction memory being positioned at crossing point of the second bit line and the third word line.~~

18. (Currently Amended) An MRAM memory array comprising:
a plurality of first and second conductive lines;
a plurality of first and second diodes, wherein each of the first diodes comprising a cathode and an anode that couples to a corresponding second conductive line and each of the second diodes comprising an anode and a cathode that couples to a corresponding first conductive line; and
a plurality of magnetic tunnel junction memories ~~each positioned where one of the first conductive lines crosses one of the second conductive lines~~, wherein each of the plurality of

magnetic tunnel junction memories is connected between a first diode at the corresponding second conductive line and a second diode at the corresponding first conductive line.

19. (Original) The MRAM memory array of claim 18 wherein each magnetic tunnel junction memories includes a pinned layer, a free layer, and a non-magnetic layer located between the pinned layer and the free layer.

20. (Original) The MRAM memory array of claim 18 wherein a total number of first and second switches is equal to a total number of first and second conductive lines.

21. (Original) The MRAM memory array of claim 18 wherein a total number of the magnetic tunnel junction memories is a product of a total number of first conductive lines and a total number of the second conductive lines.

22. (Original) The MRAM memory array of claim 18 further comprising a plurality of segments, wherein each segment includes at least two of the plurality of magnetic tunnel junction memories.

23. (Original) The MRAM memory array of claim 22 wherein the segments are separated by field effect transistors.

24. (Original) The MRAM memory array of claim 22 wherein the segments are separated by diodes.

25. (Cancelled).

REMARKS

Claims 10-14 and 17-24 are currently pending. Claims 10, 17, and 18 are amended. Reconsideration of presently pending claims 10-14 and 17-24 is respectfully requested in light of the above amendments.

Conclusion

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

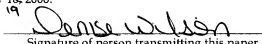
Respectfully submitted,



Wing Y Mok
Registration No. 56,237

Dated: 5/18/2006

HAYNES AND BOONE, LLP
901 Main Street, Suite 3100
Dallas, Texas 75202-3789
Telephone: 972/739-8626
Facsimile: 214/200-0853
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I hereby certify that this correspondence is being transmitted to the US Patent and Trademark Office via EFS-Web on: May 18, 2006.  Signature of person transmitting this paper
